IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the application of :

Appl. No. : 09/903,705 Confirmation No. 9187

Applicant : B. G. Goodman et al.

Filed : 07/13/2001

TC/A.U. : 2113

Examiner : Y. L. Wilson

Docket No. : TUC920000084US1

Title: FAILURE ISOLATION IN A DISTRIBUTED PROCESSING SYSTEM EMPLOYING RELATIVE LOCATION INFORMATION

DECLARATION UNDER 37 C.F.R. Section 1.132

I, **Timothy K. Pierce**, declare and say:

That I am a citizen of the United States of America and I reside at 6002 W. Bridle Way, Tucson, AZ, USA.

That I am a Firmware Engineer at IBM Corp., in the field of Data Storage Automation, since May 1979.

That I graduated in 1975 from the ITT Technical Institute, located in Indianapolis, IN, with a degree of AS in Electronics Engineering Technology.

That I am knowledgeable in the technology and science of data storage automation and embedded systems.

That I have reviewed the present U.S. Patent Application serial no. 09/903,705, and find that it describes fault detection and isolation, e.g. "isolating failures in distributed processing systems comprising processor nodes coupled by multi-drop bus networks." (page 3, lines 9-11).

"Each of a plurality of the processor nodes has information determining relative locations of the processor nodes on the multi-drop bus network, and is associated with a local error indicator. The plurality of processor nodes each independently tests access to other processor nodes on the multi-drop bus network. Upon a testing processor node detecting a failure to access at least one of the other the processor nodes, the failure detecting processor node determines, from the provided information of relative locations, the processor node having failed access which is closest to the failure detecting processor node. *** At a minimum, at least one of the processor nodes must test access to a plurality of other nodes. The failure detecting processor node stores and subsequently posts, at its associated local error indicator, an identifier of the closest processor node having failed access. A user may inspect the local error indicators and thereby isolate the detected failure, even though the failure may have been intermittent." (page 3, line 12 - page 4, line 8). (emphasis added).

The terms "location" and "relative locations" are defined throughout the specification, and are represented by the illustrations in FIGS. 4, 5 and 6.

That, I have reviewed U.S. Patent 5,884,018, Jardine et al. (Jardine), and find that it describes monitoring communication among processors in a multi-path network, and which attempts to regroup in the event of a processor communication failure, e.g. "an apparatus and protocol to determine the group of processors that will survive communications faults and/or timed-event failures in a multiprocessor system." (column 10, lines 27-31)

Jardine employs data structures, such as a matrix, that track the connectivity between the processors of the group in the multi-path network currently available to a processor.

Location or relative locations of the processors form no part of that matrix, and location or relative locations of the processors to which there is or is not communication is not even intimated. For example, Jardine states "The size of the

connectivity matrix C is NxN, where N is the number of processors #_112 in the multi-processor system. In one embodiment, each entry in the matrix is a bit, and each processor #_112 is uniquely numbered between 1 and N. An entry C(i,j) indicates the ability of processor i to receive a message from processor j." (column 13, lines 54-59).

The discussion by Jardine of the processing of the matrix C at column 19, lines 21-63, makes clear that no location or relative location information is involved in the matrix of Jardine.

The discussion by Jardine of the network characteristics at column 13, lines 8-13, makes clear that no location or relative location information would be of use in tracking the network. Unlike a multi-drop bus network for which the present '705 Application determines failures, the network of Jardine has instead "at least two paths between every pair of processors" (column 13, lines 12-13) making location or relative location of no use.

That the undersigned declares further that all statements made herein of his own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patents issuing thereon.

Further declarant saith not.

Date: 7/28/04 /s/ Timothy K. Pierce

Timothy K. Pierce